

1 We claim:

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3 1) A combiner processor comprising:

4 a sliding correlator for correlating a serial stream of
5 baseband symbols against a first codeword and forming a
6 correlation peak output;

7 a training decision function coupled to said
8 correlation peak output and generating a window output and a
9 training decision output;

10 a demultiplexer coupled to said correlation peak output
11 and having a learn control input whereby when said
12 demultiplexer learn control input is asserted:

13 said correlation peak output is coupled to a channel
14 profile memory such that said correlation peak output is
15 added to said channel profile memory when said training
16 decision output is true and said correlation peak output is
17 inverted and added to said channel profile memory when said
18 training decision is false;

19 and when said demultiplexer learn control input is not
20 asserted:

21 said correlation peak output is multiplied with the
22 complex conjugate of said channel profile memory and coupled
23 to an accumulator which adds said multiplier result during
24 each said window and generates a decision output at the end
25 of each said window.

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2 2) The combiner processor of claim 1 where said first
3 codeword is 11 bits.

4

5 3) The combiner processor of claim 1 where said first
6 codeword is a Barker codeword.

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8 4) The combiner processor of claim 1 where said first
9 codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1\}$.

10

11 5) The combiner processor of claim 1 where said first
12 codeword is $\{-1, +1, -1, -1, +1, -1, -1, -1, +1, +1, +1\}$.

13

14 6) The combiner processor of claim 1 where said serial
15 stream of baseband symbols includes Barker codewords.

16

17 7) The combiner processor of claim 1 where said serial
18 stream of baseband symbols is quadrature.

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20 8) The combiner processor of claim 7 where said serial
21 stream of quadrature symbols includes an I channel and a Q
22 channel.

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1 9) The combiner processor of claim 1 where said
2 training decision function window output has duration equal
3 to the duration of said codeword.

4

5 10) The combiner processor of claim 1 where said
6 training decision function window output includes pre-cursor
7 symbols arriving prior to the largest said correlation peak
8 in said window.

9

10 11) The combiner processor of claim 1 where said
11 training decision function window includes post-cursor
12 symbols arriving after the largest said correlation peak in
13 said window.

14

15 12) The combiner processor of claim 1 where said
16 training decision output indicates which said codeword was
17 received during said window.

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19 13) The combiner processor of claim 1 where said
20 demultiplexer learn input is asserted during a first
21 interval.

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23 14) The combiner processor of claim 13 where said first
24 interval occurs during the preamble of a received packet.

25

1 15) The combiner processor of claim 13 where said first
2 interval is greater than 10 said codeword symbols.

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4 16) The combiner processor of claim 1 where said
5 complex conjugate comprises negating the value of the Q
6 channel.

7

8 17) The combiner processor of claim 1 where said
9 channel profile memory is synchronized to said training
10 decision function window output.

11

12 18) The combiner processor of claim 1 where said
13 channel profile memory comprises a random access memory and
14 a memory controller coupled to said random access memory.

15

16 19) The combiner processor of claim 1 where said
17 channel profile memory adds quadrature said correlation peak
18 output when said demultiplexer learn input is asserted.

19

20 20) The combiner processor of claim 1 where said
21 channel profile memory is initialized when said
22 demultiplexer learn control input is first asserted.

23

1 21) The combiner processor of claim 1 where said
2 channel profile memory has a number of locations equal to
3 the number of samples in said codeword.

4
5 22) The combiner processor of claim 1 where said
6 accumulator includes a memory which is initialized at the
7 start of each said window.

8
9 23) The combiner processor of claim 1 where said
10 accumulator includes a memory and an adder which adds the
11 current said multiplier output to said memory contents.

12
13 24) The combiner processor of claim 1 where said
14 decision output compares said accumulated value against a
15 threshold at the end of said window.

16
17 25) The combiner processor of claim 24 where said
18 threshold is 0.

19
20 26) A combiner processor having two states:
21 a training state whereby a serial stream of baseband
22 symbols is correlated against a first codeword, thereby
23 producing a correlation peak output, said correlation peaks
24 examined by a training decision function to generate a
25 window output indicating the extent of said symbol and a

1 decision output which is either true or false, said
2 correlation peaks added to a channel profile memory when
3 said decision output is true and inverted and added to said
4 channel profile memory when said decision output is false;
5 a decision state whereby said serial stream of baseband
6 symbols is multiplied by the complex conjugate of the
7 contents of said channel profile memory to produce a
8 multiplier output;
9 an accumulator coupled to said multiplier output
10 whereby said adder is reset at the start of said window,
11 accumulates the output of said multiplier during said
12 window, and generates a binary output value at the end of
13 said window.

14

15 27) The combiner processor of claim 26 where said first
16 codeword is 11 bits.

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18 28) The combiner processor of claim 26 where said first
19 codeword is a Barker codeword.

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21 29) The combiner processor of claim 26 where said first
22 codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1\}$.

23

24 30) The combiner processor of claim 26 where said first
25 codeword is $\{-1, +1, -1, -1, +1, -1, -1, -1, +1, +1, +1\}$.

1

2 31) The combiner processor of claim 26 where said
3 serial stream of baseband symbols includes Barker codewords.

4

5 32) The combiner processor of claim 26 where said
6 serial stream of baseband symbols is quadrature.

7

8 33) The combiner processor of claim 32 where said
9 serial stream of quadrature symbols includes an I channel
10 and a Q channel.

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13 34) The combiner processor of claim 26 where said
14 training decision function window output has duration equal
15 to the duration of said codeword.

16

17 35) The combiner processor of claim 26 where said
18 training decision function window output includes pre-cursor
19 symbols arriving prior to the largest said correlation peak
20 in said window.

21

22 36) The combiner processor of claim 26 where said
23 training window includes post-cursor symbols arriving after
24 the largest said correlation peak in said window.

25

1 37) The combiner processor of claim 26 where said
2 training decision output indicates which said codeword was
3 received during said window.

4

5 38) The combiner processor of claim 26 where said
6 training state occurs during a first interval.

7

8 39) The combiner processor of claim 38 where said first
9 interval occurs during the preamble of a received packet.

10

11 40) The combiner processor of claim 38 where said first
12 interval is greater than 10 said codeword symbols.

13

14 41) The combiner processor of claim 26 where said
15 complex conjugate comprises negating the value of the Q
16 channel.

17

18 42) The combiner processor of claim 26 where said
19 channel profile memory is synchronized to said training
20 decision function window output.

21

22 43) The combiner processor of claim 26 where said
23 channel profile memory comprises a random access memory and
24 a memory controller coupled to said random access memory.

25

1 44) The combiner processor of claim 26 where said
2 channel profile memory adds quadrature said correlation peak
3 output when said demultiplexer learn input is asserted.

4
5 45) The combiner processor of claim 26 where said
6 channel profile memory is initialized at the beginning of
7 said training state.

8
9 46) The combiner processor of claim 26 where said
10 channel profile memory has a number of locations equal to
11 the number of samples in said codeword.

12
13 47) The combiner processor of claim 26 where said
14 accumulator includes a memory which is initialized at the
15 start of each said window.

16
17 48) The combiner processor of claim 26 where said
18 accumulator includes a memory and an adder which adds the
19 current said multiplier output to said memory contents.

20
21 49) The combiner processor of claim 26 where said
22 binary output compares said accumulated value against a
23 threshold at the end of said window.

24

1 50) The combiner processor of claim 49 where said
2 threshold is 0.

3

4 51) The combiner processor of claim 26 where said
5 decision state occurs during a second interval.

6

7 52) A process for generating a decision output from a
8 serial stream of baseband symbols, said process comprising:
9 a first learning step comprising:

10 correlating said incoming serial stream with one or
11 more codewords to generate a correlation output, examining
12 the said correlation output to generate a training decision
13 which is positive or negative, and also generating a window
14 signal indicating the start and end of said incoming
15 symbols, said incoming symbols added to a channel profile
16 memory when said training decision is positive, and
17 inverting said incoming symbols and adding to said channel
18 profile memory when said training decision is negative;

19 a second decision step comprising:

20 multiplying said correlation peaks with the complex
21 conjugate of said channel profile memory contents, thereby
22 forming a multiplier output and accumulating said multiplier
23 output during said window start time to said window end time
24 to form a decision value, and comparing said decision value
25 at the said window end time to form said decision output.

1 53) The process of claim 52 where said first codeword
2 is 11 bits.

3

4 54) The process of claim 52 where said first codeword
5 is a Barker codeword.

6

7 55) The process of claim 52 where said first codeword
8 is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1\}$.

9

10 56) The process of claim 52 where said first codeword
11 is $\{-1, +1, -1, -1, +1, -1, -1, -1, +1, +1, +1\}$.

12

13 57) The process of claim 52 where said serial stream of
14 baseband symbols includes Barker codewords.

15

16 58) The process of claim 52 where said serial stream of
17 baseband symbols is quadrature.

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19 59) The combiner processor of claim 7 where said serial
20 stream of quadrature symbols includes an I channel and a Q
21 channel.

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24 60) The process of claim 52 where said window output
25 has duration equal to the duration of said codeword.

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2 61) The process of claim 52 where said window output
3 includes pre-cursor symbols arriving prior to the largest
4 said correlation peak in said window.

5

6 62) The process of claim 52 where said window includes
7 post-cursor symbols arriving after the largest said
8 correlation peak in said window.

9

10 63) The process of claim 52 where said training
11 decision output indicates which said codeword was received
12 during said window.

13

14 64) The process of claim 52 where said learning step
15 precedes said decision step.

16

17 65) The process of claim 52 where said learning step
18 occurs during the preamble of a received packet.

19

20 66) The process of claim 52 where said learning step
21 uses more than 10 said codeword symbols.

22

23 67) The process of claim 52 where said complex
24 conjugate comprises negating the value of the Q channel.

25

1 68) The process of claim 52 where said channel profile
2 memory is synchronized to said window.

3
4 69) The process of claim 52 where said channel profile
5 memory comprises a random access memory and a memory
6 controller coupled to said random access memory.

7
8 70) The process of claim 52 where said channel profile
9 memory adds quadrature said correlation peak output during
10 said learning step.

11
12 71) The process of claim 52 where said channel profile
13 memory is initialized at the beginning of said learning
14 step.

15
16 72) The process of claim 52 where said channel profile
17 memory has a number of locations equal to the number of
18 samples in said codeword.

19
20 73) The process of claim 52 where said accumulation
21 includes a memory which is initialized at the start of each
22 said window.

1 74) The process of claim 52 where said accumulation
2 includes a memory and an adder which adds the current said
3 multiplier output to said memory contents.

4
5 75) The process of claim 52 where said decision value
6 compares said accumulated value against a threshold at the
7 end of said window.

8
9 76) The combiner processor of claim 24 where said
10 threshold is 0.

11
12
13 77) A combiner processor comprising:
14 a sliding correlator for correlating a serial stream of
15 baseband symbols against a first codeword and forming a
16 correlation peak output;
17 a training decision function coupled to said
18 correlation peak output and generating a window output and a
19 training decision output;
20 said correlation peak output is coupled to a channel
21 profile memory such that said correlation peak output is
22 added to said channel profile memory when said training
23 decision output is true and said correlation peak output is
24 inverted and added to said channel profile memory;

1 a decision control input whereby when said decision
2 control input is asserted, said correlation peak output is
3 multiplied with the complex conjugate of said channel
4 profile memory and coupled to an accumulator which adds said
5 multiplier result during each said window and generates a
6 decision output at the end of each said window.

7
8 78) The combiner processor of claim 77 where said first
9 codeword is 11 bits.

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11 79) The combiner processor of claim 77 where said first
12 codeword is a Barker codeword.

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14 80) The combiner processor of claim 77 where said first
15 codeword is $\{+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1\}$.

16
17 81) The combiner processor of claim 77 where said first
18 codeword is $\{-1, +1, -1, -1, +1, -1, -1, -1, +1, +1, +1\}$.

19
20 82) The combiner processor of claim 77 where said
21 serial stream of baseband symbols includes Barker codewords.

22
23 83) The combiner processor of claim 77 where said
24 serial stream of baseband symbols is quadrature.

1 84) The combiner processor of claim 7 where said serial
2 stream of quadrature symbols includes an I channel and a Q
3 channel.

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6 85) The combiner processor of claim 77 where said
7 training decision function window output has duration equal
8 to the duration of said codeword.

9
10 86) The combiner processor of claim 77 where said
11 training decision function window output includes pre-cursor
12 symbols arriving prior to the largest said correlation peak
13 in said window.

14
15 87) The combiner processor of claim 77 where said
16 training decision function window includes post-cursor
17 symbols arriving after the largest said correlation peak in
18 said window.

19
20 88) The combiner processor of claim 77 where said
21 training decision output indicates which said codeword was
22 received during said window.

23
24 89) The combiner processor of claim 77 where said
25 decision input is not asserted during a first interval.

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2 90) The combiner processor of claim 89 where said first
3 interval occurs during the preamble of a received packet.

4

5 91) The combiner processor of claim 89 where said first
6 interval is greater than 10 said codeword symbols.

7

8 92) The combiner processor of claim 77 where said
9 complex conjugate comprises negating the value of the Q
10 channel.

11

12 93) The combiner processor of claim 77 where said
13 channel profile memory is synchronized to said training
14 decision function window output.

15

16 94) The combiner processor of claim 77 where said
17 channel profile memory comprises a random access memory and
18 a memory controller coupled to said random access memory.

19

20 95) The combiner processor of claim 77 where said
21 channel profile memory adds quadrature said correlation peak
22 output at all times.

23

24 96) The combiner processor of claim 77 where said
25 channel profile memory is initialized.

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2 97) The combiner processor of claim 77 where said
3 channel profile memory has a number of locations equal to
4 the number of samples in said codeword.

5

6 98) The combiner processor of claim 77 where said
7 accumulator includes a memory which is initialized at the
8 start of each said window.

9

10 99) The combiner processor of claim 77 where said
11 accumulator includes a memory and an adder which adds the
12 current said multiplier output to said memory contents.

13

14 100) The combiner processor of claim 77 where said
15 decision output compares said accumulated value against a
16 threshold at the end of said window.

17

18 101) The combiner processor of claim 100 where said
19 threshold is 0.

20

21 102) The combiner processor of claim 1 where said
22 codewords are used for direct sequence spread spectrum
23 communications.

24

1 103) The combiner processor of claim 26 where said
2 codewords are used for direct sequence spread spectrum
3 communications.

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6 104) The combiner processor of claim 52 where said
7 codewords are used for direct sequence spread spectrum
8 communications.

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11 105) The combiner processor of claim 77 where said
12 codewords are used for direct sequence spread spectrum
13 communications.